WHAT IS CLAIMED IS:

1. A logic circuit comprising:

a dynamic logic portion for evaluating a Boolean function of one or more input signals, wherein a logic signal on a dynamic node, asserted in response to a first logic state of a first clock signal or a first logic state of a feedback signal, comprises either a logic true or a logic false Boolean combination of the one or more input signals and wherein the dynamic node is pre-charged to the first logic state corresponding to the logic false Boolean combination of the one or more input signals when the one or more input signals have any of possible logic false Boolean combinations; and

a static portion coupled to the dynamic node and generating the feedback signal in response to the logic signal and generating a latched data output signal in response to the logic signal and a second clock signal.

2. The logic circuit of claim 1 further generating an inverted data output signal as the logic inversion of the latched data output signal.

3. The logic circuit of claim 1, wherein the first clock signal and the second clock signal are the same signal.

4. The logic circuit of claim 1, wherein the feedback signal is the latched data output signal

5. The logic circuit of claim 1, wherein the feedback signal is generated as a logic inversion of the logic signal.

6. The logic circuit of claim 1, wherein the dynamic portion comprises:

an inverting complementary logic circuit having a first power node coupled to first power supply voltage, an evaluate node, one or more inputs receiving the one or more input signals, and the dynamic node; and

an evaluate circuit having a clock node receiving the first clock signal, a feedback node receiving the feedback signal, a second power node coupled to a second power supply voltage, and a common node coupled to the evaluate node.

7. The logic circuit of claim 6, wherein the inverting complementary logic comprises:

one or more PFETs each having a source, a drain, and a gate coupled to a corresponding one of the plurality of input signals, wherein at least one PFET source of the one or more PFETs is coupled to the first power node, at least one PFET drain of the one or more PFETs is coupled to the dynamic node and the one or more PFETs couple the first power node to the dynamic node in response to a logic false Boolean combination of the one or more input signals; and

one or more NFETs each having a source, a drain, and a gate coupled to a corresponding one of the plurality of input signals, wherein at least one NFET drain of the one or more NFETs is coupled to the dynamic node, at least one of the NFET source of the one or more NFETs is coupled to the evaluate node and the one or more NFETs couple the dynamic node to the evaluate node in response to a logic true Boolean combination of the one or more input signals.

8. The logic circuit of claim 7, wherein the evaluate circuit comprises:

a first NFET having a source coupled to the second power supply node, a drain coupled to the common node and a gate coupled to the first clock signal; and

a second NFET having a source coupled to the second power supply node, a drain coupled to the common node, and a gate coupled to the latched data output signal.

9. The logic circuit of claim 7, wherein the evaluate circuit comprises:

a first NFET having a source coupled to the second power supply node, a drain coupled to the common node and a gate coupled to the first clock signal;

a second NFET having a source coupled to the second power supply node, a drain coupled to the common node and a gate; and

an inverter having an input coupled to the dynamic node and an output coupled to the gate of the second NFET.

10. The logic of claim 2 wherein the static portion includes:

a first PFET having a gate coupled to the dynamic node, a source coupled to the first power supply voltage and a drain;

a first NFET having a gate coupled to the gate of the first PFET, a drain coupled to the drain of the first PFET forming a data output node generating the latched data output signal, and a source;

a second NFET having a gate coupled to the second clock signal, a source coupled to the second power supply voltage and a drain coupled to the source of the first NFET;

a third NFET having a drain coupled to the drain of the second NFET, a source coupled to the second power supply voltage and a gate;

an inverting circuit having an input coupled to the data output node, an output node coupled to the gate of the third NFET and generating the inverting data output signal; and

a second PFET having a gate coupled to the output node of the inverting circuit, a drain coupled to the data output node, and a source coupled to the first power supply voltage.

11. A data processing system comprising:

a central processing unit (CPU); and

a memory operable for communicating instructions and operand data to said CPU, wherein said CPU includes a logic system having a logic circuit with a dynamic logic portion for evaluating a Boolean function of one or more input signals, wherein a logic signal on a dynamic node, asserted in response to a first logic state of a first clock signal or the first logic state of a feedback signal, comprises either a logic true or a logic false Boolean combination of the one or more input signals and wherein the dynamic node is pre-charged to the first logic state corresponding to the logic false Boolean combination of the one or more input signals when the one or more input signals have any of possible logic false Boolean combinations; and a static portion coupled to the dynamic node and generating the feedback signal in response to the logic signal and generating a latched data output signal in response to the logic signal and a second clock signal.

12. The data processing system of claim 11 further generating an inverted data output signal as the logic inversion of the latched data output signal.

13. The data processing system of claim 11, wherein the first clock signal and the second clock signal are the same signal.

14. The data processing system of claim 11, wherein the feedback signal is the latched data output signal

15. The data processing system of claim 11, wherein the feedback signal is generated as a logic inversion of the logic signal.

16. The data processing system of claim 11, wherein the dynamic portion comprises:

an inverting complementary logic circuit having a first power node coupled to first power supply voltage, an evaluate node, one or more inputs receiving the one or more input signals, and the dynamic node; and

an evaluate circuit having a clock node receiving the first clock signal, a feedback node receiving the feedback signal, a second power node coupled to a second power supply voltage, and a common node coupled to the evaluate node.

17. The data processing system of claim 16, wherein the inverting complementary logic comprises:

one or more PFETs each having a source, a drain, and a gate coupled to a corresponding one of the plurality of input signals, wherein at least one PFET source of the one or more PFETs is coupled to the first power node, at least one PFET drain of the one or more PFETs is coupled to the dynamic node and the one or more PFETs couple the first power node to the dynamic node in response to a logic false Boolean combination of the one or more input signals; and

one or more NFETs each having a source, a drain, and a gate coupled to a corresponding one of the plurality of input signals, wherein at least one NFET drain of the one or more NFETs is coupled to the dynamic node, at least one of the NFET source of the one or more NFETs is coupled to the evaluate node and the one or more NFETs couple the dynamic node to the evaluate node in response to a logic true Boolean combination of the one or more input signals.

18. The data processing system of claim 17, wherein the evaluate circuit comprises:

a first NFET having a source coupled to the second power supply node, a drain coupled to the common node and a gate coupled to the first clock signal; and

a second NFET having a source coupled to the second power supply node, a drain coupled to the common node, and a gate coupled to the latched data output signal.

19. The data processing system of claim 17, wherein the evaluate circuit comprises:

a first NFET having a source coupled to the second power supply node, a drain coupled to the common node and a gate coupled to the first clock signal;

a second NFET having a source coupled to the second power supply node, a drain coupled to the common node and a gate; and

an inverter having an input coupled to the dynamic node and an output coupled to the gate of the second NFET.

20. The logic of claim 12 wherein the static portion includes:

a first PFET having a gate coupled to the dynamic node, a source coupled to the first power supply voltage and a drain;

a first NFET having a gate coupled to the gate of the first PFET, a drain coupled to the drain of the first PFET forming a data output node generating the latched data output signal, and a source;

a second NFET having a gate coupled to the second clock signal, a source coupled to the second power supply voltage and a drain coupled to the source of the first NFET;

a third NFET having a drain coupled to the drain of the second NFET, a source coupled to the second power supply voltage and a gate;

an inverting circuit having an input coupled to the data output node, an output node coupled to the gate of the third NFET and generating the inverting data output signal; and

a second PFET having a gate coupled to the output node of the inverting circuit, a drain coupled to the data output node, and a source coupled to the first power supply voltage.